

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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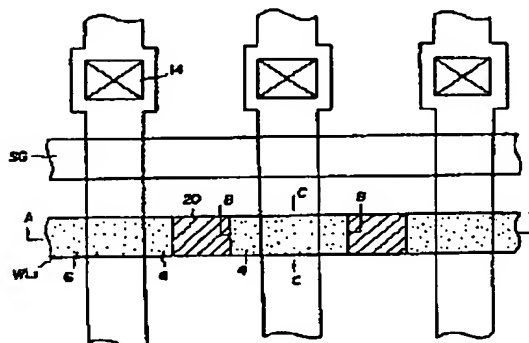
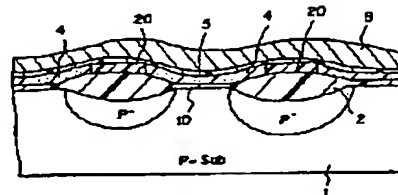
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APPLICANT : TOSHIBA CORP;

INVENTOR : KIRISAWA RYOHEI;

INT.CL. : H01L 29/788 H01L 27/115 H01L 29/792

TITLE : NON-VOLATILE SEMICONDUCTOR  
STORAGE DEVICE AND  
MANUFACTURE THEREOF



ABSTRACT : PURPOSE: To prevent a field inversion when a high voltage is applied for increasing a reliability of the device by locating an insulated film between floating gates which adjoin each other for increasing substantially the thickness of the element isolation insulated film in such a structure that at least two memory transistors are formed with an element isolation region located between.

CONSTITUTION: A NAND-type cell EEPROM is constituted of a MOS transistor section which composes three adjoining selection gates on the bit line side and a MOS transistor section which composes three memory cells. Under an element isolation insulated film 2, a p-type layer 14 is formed for preventing an inversion. In this EEPROM, an insulated film 20 or a silicon oxide film is selectively formed between floating gates 4 which adjoin each other. Consequently, the element isolation insulated film 2 under a control gate becomes (substantially thick and a field inversion voltage can be increased. Even when a high voltage is applied to the control gate, a field inversion is avoided and thus the device can be made a more integrated and highly reliable one.

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